THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte STEVEN K. HELLER and ANDREW SHAW

Appeal No. 96-3697
Application No.08/255,304[1]

ON BRIEF

Before URYNOWICZ, JERRY SMITH, and FRAHM, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 1-14, all the claims pending in the application.

The invention pertains to a system for generating a

[1] Application for patent filed June 7, 1994. According to appellants, this application is a continuation of Application 07/857,545, filed March 25, 1992, now abandoned.

program to effect a reassignment of data items. Claim 1 is illustrative and reads as follows:

> For use in connection with a computer system having a plurality of processing elements, each including a memory, each memory including a plurality of storage locations for storing a data item, each storage location within the computer being identified by an address comprising a plurality of address bits assigned to a corresponding plurality of address bit positions, a selected number of said address bit positions constituting a global portion and others of said address bit positions constituting a local portion, with the address bits in the address bit positions of the global portion of an address identifying a processing element and the address bits in the address bits of the local portion of the address identifying a storage location within the memory of the processing element identified by the address bits in address bit positions of the global portion, a system for generating a program to facilitate use of a predetermined set of tools to effect a reassignment of data items among processing elements and storage location to, in turn, provide a predetermined rearrangement of address bit positions from an initial arrangement of address bit positions to a final arrangement of address bit positions, said system comprising:
>
> a global processing portion for generating a global program portion of said program to enable use of said tools to effect a reassignment of data items as among said processing elements to, in turn, effect a rearrangement of address bits in address bit positions from said initial arrangement to an intermediate arrangement in which the address bit positions in the global portion correspond to the global portion of the final arrangement; and
>
> B. a local processing portion for generating a

local program portion of said program to enable use of said tools to effect a reassignment of data items as among storage locations within said processing elements to, in turn, effect a rearrangement of the address bits in address bit positions in the local portion of the intermediate arrangement to the final arrangement.

The references relied upon by the examiner as evidence of obviousness are:

Robinson et al. (Robinson) 5,237,691 Aug. 17, 1993
(filed Aug. 1, 1990)

"Optimal Matrix Transposition and Bit Reversal on Hypercubes: All-to-All Personalized Communication," Journal of Parallel and Distributed Computing, 1991 (Edelman).

The appealed claims stand rejected under 35 U.S.C. § 103 as being unpatentable over Edelman in view of Robinson.

The respective positions of the examiner and the appellants with regard to the propriety of the rejection are set forth in the final rejection (Paper No. 21) and the examiner's answer (Paper No. 30) and the appellants' brief (Paper No. 29).

Appellants' Invention

The invention is an arrangement for generating a

program for enabling a parallel computer to use various tools to transfer data among processors of the computer to effect a rearrangement of address bits in the addresses of the data stored in the processors' memories. By way of example, one of the tools is the "all-to-all personalized communication" tool (AAPC) which is described in the Edelman reference. The AAPC tool enables a

reassignment of data among storage locations of the various

processors to effect a rearrangement of address bits between global and local bit locations.

Each processor includes a memory having a plurality of storage locations, each location identified by a local address having a particular encoding of a set of local address bits. Each processor is identified by a global address having an encoding of global address bits. Each storage location in the parallel computer is identified by the combination of the local and global address bits. For example, if there are "J" address bits in bit locations $a_{J-1 \ldots} a_{0,}$ the bits in bit locations

$a_{J-1\ldots}a_K$ (J-1>K>0) may comprise the global bits identifying the processor, and bits in bit locations $a_{K-1\ldots}a_0$ are local address bits identifying the particular storage location. The complete address would be represented by bits in bit locations $a_{J-1}\ldots a_K$ $a_{K-1\ldots}a_{0.}$

During data processing, it may be necessary to reassign the data among the various processors' storage locations in a selected way by a rearrangement of address bits among the various address bit locations. For example, a transpose operation would be represented by interchanging global address bits and local address bits. The addresses for the transposed data would be $a_{K-1}\ldots a_0$ $a_{J-1}\ldots a_K$.

The Prior Art

Edelman discloses the AAPC tool referred to in the above discussion of appellants' invention.

Robinson discloses a system and method for generating computer programs for use in parallel processor arrangements from a user generated block diagram of the program.

The Rejection under 35 U.S.C. § 103

Appellants have not specifically argued the patentability of claims 2-14, indicating how they define appellants' invention over the prior art. Accordingly, claims 2-14 stand or fall with independent claim 1. In re Nielson, 816 F.2d 1567, 1570, 2 USPQ2d 1525, 1526-27 (Fed. Cir. 1987).

With respect to claim 1, the examiner's position is that Edelman discloses a processing array wherein the system comprises addresses having a global portion (node address) and a local portion (page 1, col. 1). The reassignment of data items correlates to the transposing process. The intermediate arrangement is the address as it exists after the initial

transpose (page 1, col. 1) and before its arrival at the final destination. The system for generating a program correlates to the algorithm. The examiner asserts that Robinson discloses a system for generating a program for data reassignment (col. 7, line 44, et seq.) and that it would have been obvious for one of ordinary skill in the art at the time the invention was made to incorporate Robinson's program generation system into the Edelman system because Robinson's program generation would allow for data reassignment among processing elements in the Edelman system.

In their brief, appellants argue that Edelman does not teach or suggest the invention recited in claim 1. It is argued that the reference merely discloses a tool, identified as "All-to-All Personalized Communication", which may be called by a program that would be generated by the system in claim 1 and that the reference does not disclose a system for generating such a program. It is further argued that Edelman discloses a tool for rearranging address bits as between a global address portion and a local address portion but not for

rearranging address bits within the global address portion or the local address portion.

Appellants argue that Robinson does not teach or suggest the invention recited in claim 1. The contention is made that there is no suggestion in Robinson that dataform modules generate programs in response to an initial address bit ordering and a final address bit ordering to enable use of one or more tools to perform a data reassignment among processing elements and storage locations to effect a rearrangement of address bits. Appellants urge that Robinson's system does not automatically generate a program using a selected set of tools for effecting the reassignment of data items to effect a selected rearrangement of data bits.

Lastly, appellants argue that the combination of Edelman and Robinson fails to teach or suggest the global and local address portions recited in claim 1.

In response to appellants' arguments, the examiner asserts appellants' rearrangement of address bits is functionally equivalent to the swapping of addresses as

disclosed in Edelman in that both result in the processing element having a different address. With respect to Robinson, it is urged that the reference discloses a system for generating a program to enable use of one or more tools for performing rearrangement of data. In support of this position, the examiner draws attention to Robinson's disclosure at column 1, line 37, et seq., wherein a program is generated to use the interface modules which perform the rearrangement of the data, and column 7, line 44, et seq. Lastly, the observations are made that neither generation of a program in response to an initial address bit ordering and a final address bit ordering nor automatic generation of a program using a selected set of tools for effecting a reassignment of data items are required by claim 1.

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that the rejection should not be sustained. The

examiner's position that appellants' rearrangement of address bits is functionally equivalent to the swapping of addresses as disclosed in Edelman in that both result in the processing element having a different address does not establish the obviousness of claim 1 over Edelman and Robinson. Neither reference has been shown to teach rearrangement of data items as among processing elements or storage locations within processing elements, nor has it been shown that it would have been obvious to one of ordinary skill in the art at the time the invention was made to so modify the teachings of the combined art. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-1784 (Fed. Cir. 1992).

Although we will not sustain the rejection of claims 1-14 for the above reason, we agree with the examiner that claim 1 does not require that a program be generated in response to an initial address bit ordering and a final address bit ordering, and that the claim does not require a system that automatically generates a program. Additionally, appellants' argument that Edelman does not disclose a system

for generating a program is not persuasive because, as noted by the examiner, Robinson teaches such a system.

REVERSED

STANLEY M. URYNOWICZ, JR. Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ERIC S. FRAHM Administrative Patent Judge	)	

SMU/dal

Appeal No. 96-3697
Serial No. 08/255,304

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